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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,338	02/12/2004	Rajesh Kumar	01-549	1775

23400 7590 10/18/2005

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/776,338	KUMAR ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *4,6,7 and 10-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☒ Claim(s) *5,8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election with traverse of Species I (claims 1-3, 5 and 8-9) in the reply filed on 8/9/05 is acknowledged. The traversal is on the ground(s) that Applicant elects with traverse. This is not found persuasive because Applicant did not distinctly and specifically point out the supposed errors in the restriction requirement. The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yonemaru (US. 2002/0070409) in view of Majumdar et al (US. 2004/0070047).

Yonemaru (Fig. 1C) discloses a semiconductor device comprising: a first field effect transistor m1b including a source and a gate and disposed in a silicon substrate (see Fig. 3); and a second field effect transistor m1a including a drain and a gate and disposed in the substrate, wherein the drain of the second field effect transistor m1a connects to the source of the first field transistor m1b, and wherein the gate of the second field effect transistor m1a connects to the gate of the first field effect transistor m1b (See Fig. 1C and par. [0092]).

Yonemaru does not disclose the first and second transistors disposed in the substrate made of silicon carbide.

However, Majumdar (Fig. 1) discloses the forming of a first field effect transistor 101 and a second field effect transistor 102 in a silicon carbide substrate (11,12) (par. [0041]). Accordingly, it would have been obvious to form the first and second field effect transistors of Yonemaru in the substrate made of silicon carbide because the silicon carbide substrate would increase the breakdown voltage and the band gap of the device, as taught by Majumdar (par. [0012]).

4. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonemaru and Majumdar as applied to claim 1 above and further in view of Baliga (US. 5,396,085).

Regarding claim 2, neither Yonemaru nor Majumdar discloses the connections between a metal-oxide semiconductor field-effect transistor and the second field effect transistor as claimed.

However, Baliga (Fig. 5A and 6) discloses a semiconductor device comprising: a metal-oxide semiconductor field-effect transistor 12 (or 50 in Fig. 6) including a drain and a source and disposed in a silicon substrate (column 6, lines 54-58); and a field effect transistor 22 (or 46) including a drain and a source and disposed in a silicon carbide substrate (column 7, lines 1-5), wherein the drain 16 of the metal-oxide semiconductor field-effect transistor 12 connects to the source 24 of the field effect transistor 22, and wherein the source 14 of the metal-oxide semiconductor field-effect

transistor 12 connects to the gate 28 of the field effect transistor 22. Accordingly, it would have been obvious to provide a metal-oxide semiconductor field-effect transistor having drain and source respectively connecting to the source and gate of the second field-effect transistor m1a of Yonemaru in order to provide a three-terminal silicon carbide switching device with rectifying gate, as taught by Baliga (column 6, lines 50-52).

Regarding claim 3, Baliga (Fig. 5A) further teaches that the metal-oxide semiconductor field-effect transistor 12 (or 50 in Fig. 6) is turned-on by applying a positive gate voltage to the gate electrode (column 7, lines 42-50). Therefore, it would have been obvious to apply a gate voltage in a range between 5 and 10 volts to the gate electrode of the metal-oxide semiconductor field-effect transistor because such voltage levels are commonly used for turn-on the transistor.

Allowable Subject Matter

5. Claims 5 and 8-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose all the limitations recited in the dependent claims 5 and 8-9. Specifically, the prior art of record fails to disclose the structures and the arrangements of a vertical junction field effect transistor and a lateral junction field effect transistor as claimed.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
October 17, 2005

PHAT X. CAO
PRIMARY EXAMINER